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REVISION HISTORY

Version	Date	Page	Description
2.1	Jan.21, 2013	All	Spec Ver.2.1 was first issued.

1. GENERAL DESCRIPTION

1.1 OVERVIEW

N133BGE-EB1 is a 13.3" (13.3" diagonal) TFT Liquid Crystal Display module with LED Backlight unit and 30 pins eDP interface. This module supports 1366 x 768 HD mode and can display 262,144 colors. The optimum viewing angle is at 6 o'clock direction.

1.2 GENERAL SPECIFICATIONS

Item	Specification	Unit	Note
Screen Size	13.3 diagonal	inch	
Driver Element	a-si TFT active matrix	-	-
Pixel Number	1366 x R.G.B. x 768	pixel	-
Pixel Pitch	0.2148 (H) x 0.2148 (V)	mm	-
Pixel Arrangement	RGB vertical stripe	-	-
Display Colors	262,144	color	-
Transmissive Mode	Normally white	-	-
Surface Treatment	Hard coating (3H)	-	-
Luminance, White	300	Cd/m2	
Power Consumption	Total 1.98W (Max.) @ cell 0.71W (Max.), BL 1.27W (Max.)		(1)

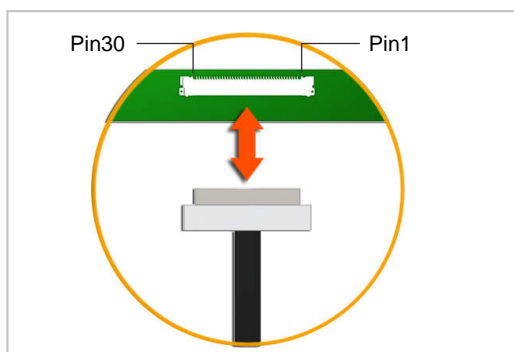
Note (1) The specified power consumption (with converter efficiency) is under the conditions at VCCS = 3.3 V, $f_v = 60$ Hz, LED_VCCS = Typ, $f_{PWM} = 200$ Hz, Duty=100% and $T_a = 25 \pm 2$ °C, whereas mosaic pattern is displayed.

2. MECHANICAL SPECIFICATIONS

Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal (H)	305.8	306.3	306.8	mm	(1)
	Vertical (V)	177.2	177.7	178.2	mm	
	Thickness (T)		2.668	2.85	mm	
Bezel Area	Horizontal	296.17	296.42	296.77	mm	
	Vertical	167.77	167.97	168.17	mm	
Active Area	Horizontal	293.32	293.42	293.52	mm	
	Vertical	164.87	164.97	165.07	mm	
Weight		-	224.5	240	g	

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

2.1 CONNECTOR TYPE



Please refer Appendix Outline Drawing for detail design.

Connector Part No.: IPEX: 20455-030E-12, TYCO: 5-2069716-2

User's connector Part No: IPEX-20453-030T- 03 , TYCO: 5-2069715-2

3. ABSOLUTE MAXIMUM RATINGS

3.1 ABSOLUTE RATINGS OF ENVIRONMENT

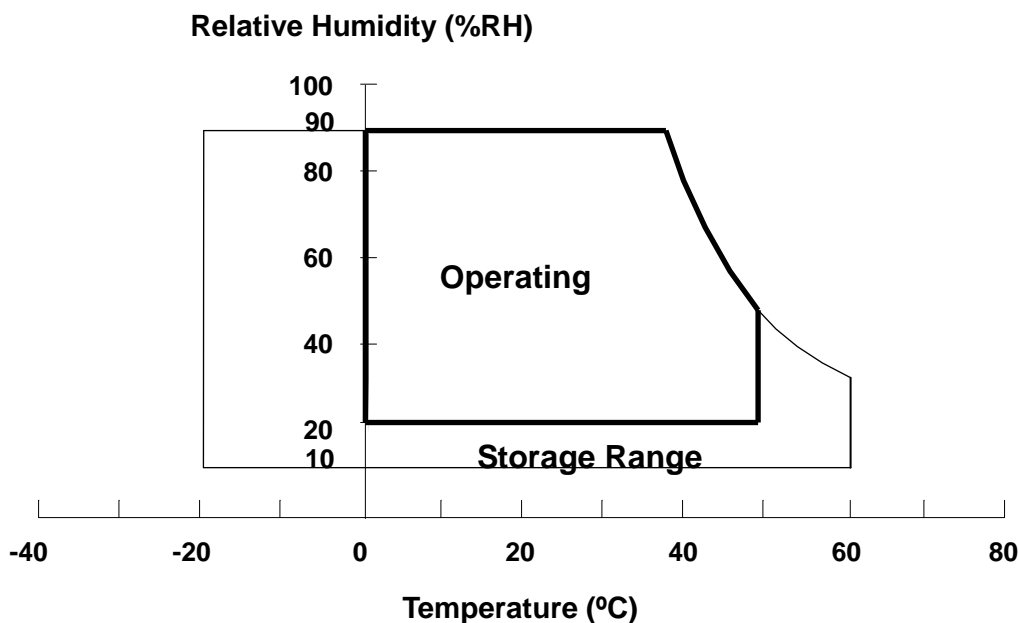
Item	Symbol	Value		Unit	Note
		Min.	Max.		
Operating Ambient Temperature	T _{OP}	0	+50	°C	
Operating Temperature for Panel	-	0	+60	°C	
Storage Temperature	T _{STG}	-20	+60	°C	
Operating Ambient Humidity	H _{OP}	20	90	%RH	
Storage Humidity	H _{STG}	10	90	%RH	
Air Pressure		70		KPa	Operation
Air Pressure		12		KPa	Non-Operation
Altitude			4572	m	Operation
Altitude			15240	m	Non-Operation

Note (1) (a) 90 %RH Max. (Ta <= 40 °C).

(b) Wet-bulb temperature should be 39 °C Max. (Ta > 40 °C).

(c) No condensation.

Note (2) The temperature of panel surface should be 0 °C min. and 60 °C max.



3.2 ELECTRICAL ABSOLUTE RATINGS

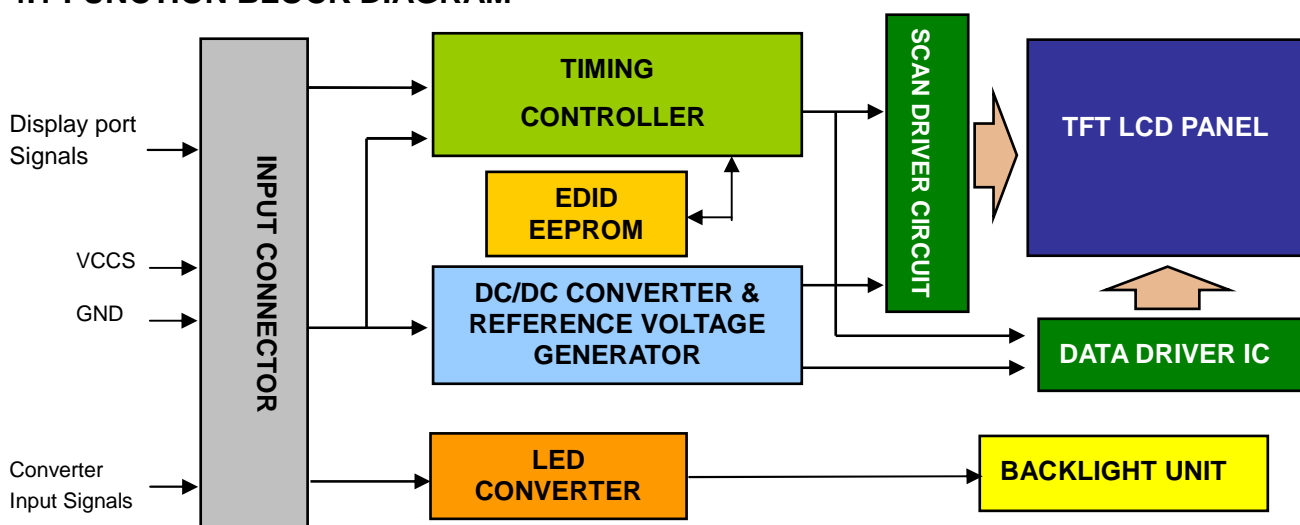
3.2.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	VCCS	-0.3	+4.0	V	(1)
Logic Input Voltage	V _{IN}	-0.3	VCCS+0.3	V	
Converter Input Voltage	LED_VCCS	-0.3	26	V	(1)
Converter Control Signal Voltage	LED_PWM,	-0.3	5	V	(1)
Converter Control Signal Voltage	LED_EN	-0.3	5	V	(1)

Note (1) Stresses beyond those listed in above "ELECTRICAL ABSOLUTE RATINGS" may cause permanent damage to the device. Normal operation should be restricted to the conditions described in "ELECTRICAL CHARACTERISTICS".

4. ELECTRICAL SPECIFICATIONS

4.1 FUNCTION BLOCK DIAGRAM



4.2. INTERFACE CONNECTIONS

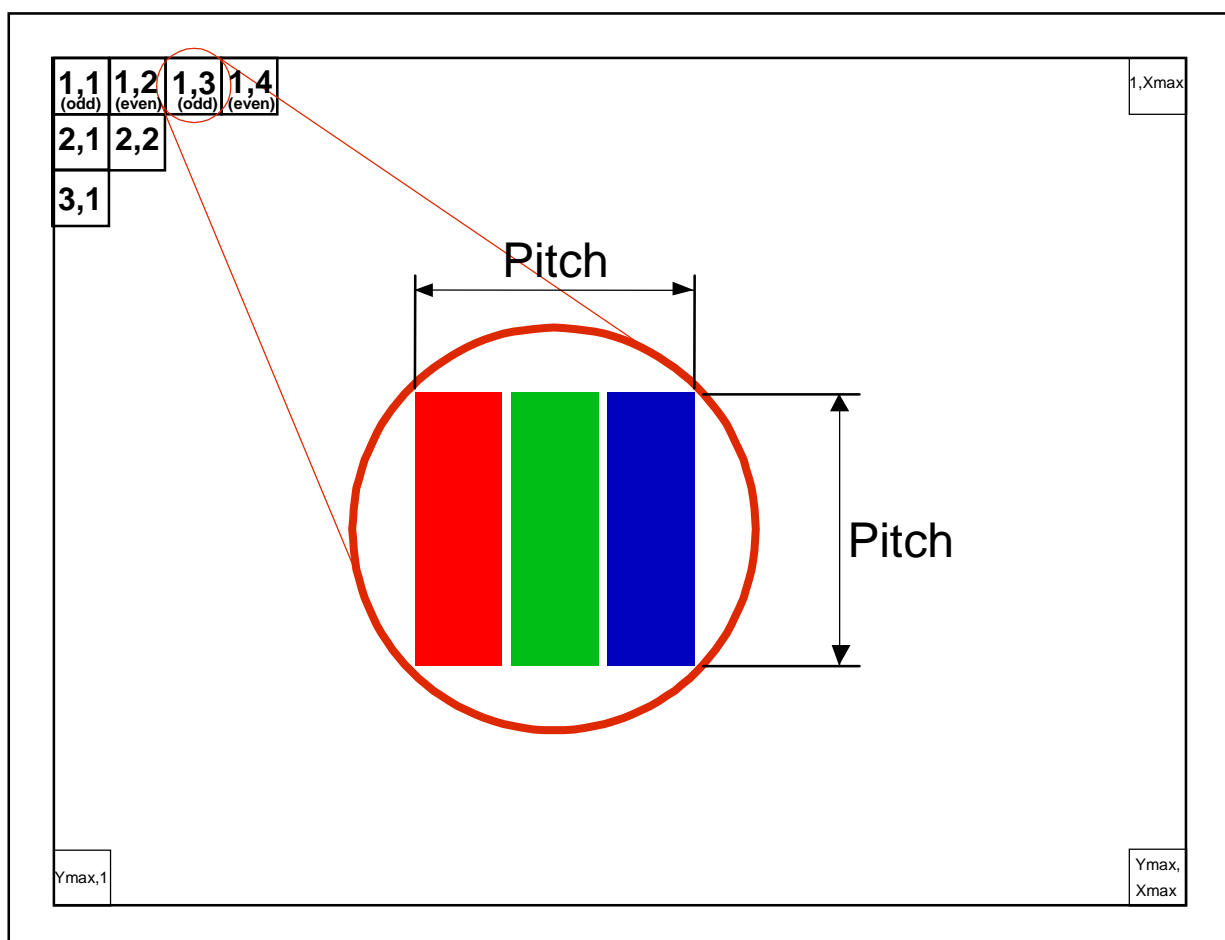
PIN ASSIGNMENT

Pin	Symbol	Description	Remark
1	NC	No Connection (Reserved)	
2	H_GND	High Speed Ground	
3	NC	No Connection (Reserved)	
4	NC	No Connection (Reserved)	
5	H_GND	High Speed Ground	
6	ML0-	Complement Signal-Lane 0	
7	ML0+	True Signal-Main Lane 0	
8	H_GND	High Speed Ground	
9	AUX+	True Signal-Auxiliary Channel	
10	AUX-	Complement Signal-Auxiliary Channel	
11	H_GND	High Speed Ground	
12	VCCS	Power Supply +3.3 V (typical)	
13	VCCS	Power Supply +3.3 V (typical)	
14	NC	No Connection (Reserved for CMI test)	
15	GND	Ground	
16	GND	Ground	
17	HPD	Hot Plug Detect	
18	BL_GND	BL Ground	
19	BL_GND	BL Ground	
20	BL_GND	BL Ground	
21	BL_GND	BL Ground	
22	LED_EN	BL_Enable Signal of LED Converter	
23	LED_PWM	PWM Dimming Control Signal of LED Converter	
24	NC	No Connection	

25	NC	No Connection	
26	LED_VCCS	BL Power	
27	LED_VCCS	BL Power	
28	LED_VCCS	BL Power	
29	LED_VCCS	BL Power	
30	NC	No Connection (Reserved)	

Note (1) The first pixel is odd as shown in the following figure.

(2) Connector Part No.: IPEX: 20455-030E-12, TYCO: 5-2069716-2



4.3 ELECTRICAL CHARACTERISTICS

4.3.1 LCD ELECTRONICS SPECIFICATION

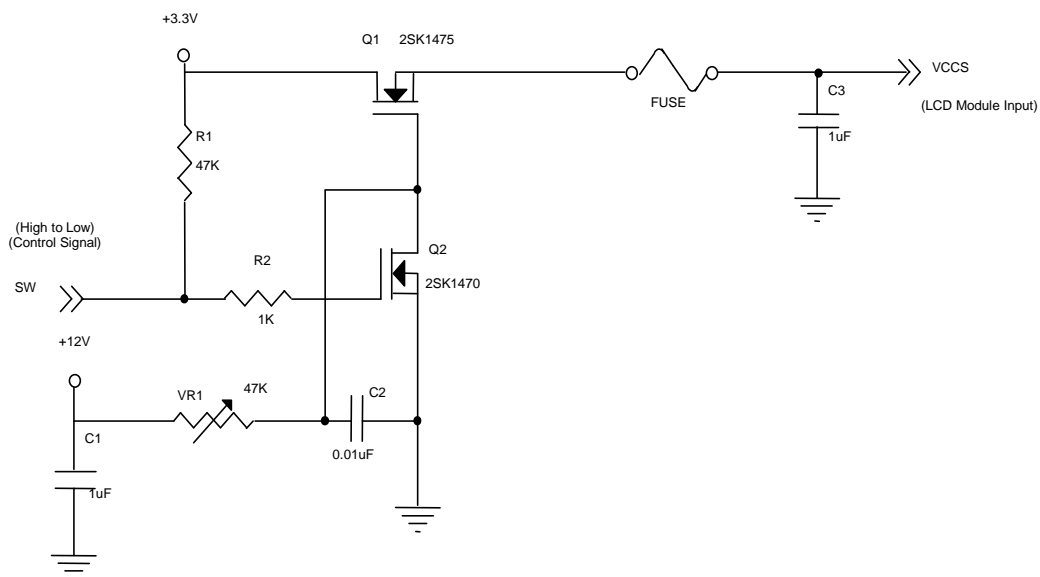
Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		VCCS	3.0	3.3	3.6	V	(1)-
HPD	High Level		2.25	-	2.75	V	
	Low Level		0	-	0.4	V	
Ripple Voltage		V_{RP}	-	50	-	mV	(1)-
Inrush Current		I_{RUSH}	-	-	1.5	A	(1),(2)
Power Supply Current	Mosaic	I_{CC}		190	215	mA	(3)a
	Black			210	230	mA	(3)

Note (1) The ambient temperature is $T_a = 25 \pm 2 \text{ }^\circ\text{C}$.

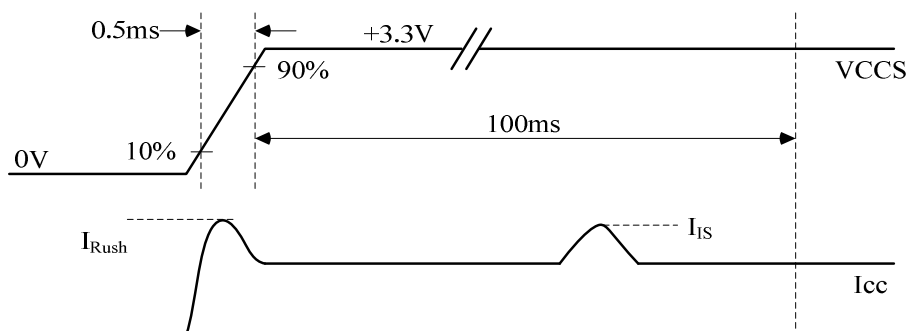
Note (2) I_{RUSH} : the maximum current when VCCS is rising

I_{IS} : the maximum current of the first 100ms after power-on

Measurement Conditions: Shown as the following figure. Test pattern: black.

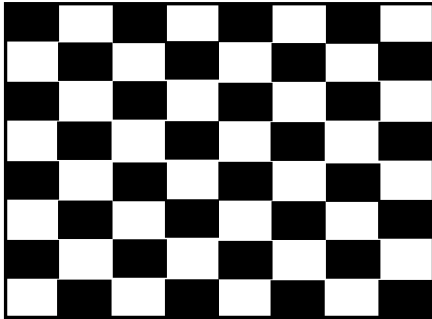


VCCS rising time is 0.5ms



Note (3) The specified power supply current is under the conditions at $V_{CCS} = 3.3\text{ V}$, $T_a = 25 \pm 2\text{ }^\circ\text{C}$, DC Current and $f_v = 60\text{ Hz}$, whereas a power dissipation check pattern below is displayed.

a. Mosaic Pattern



Active Area

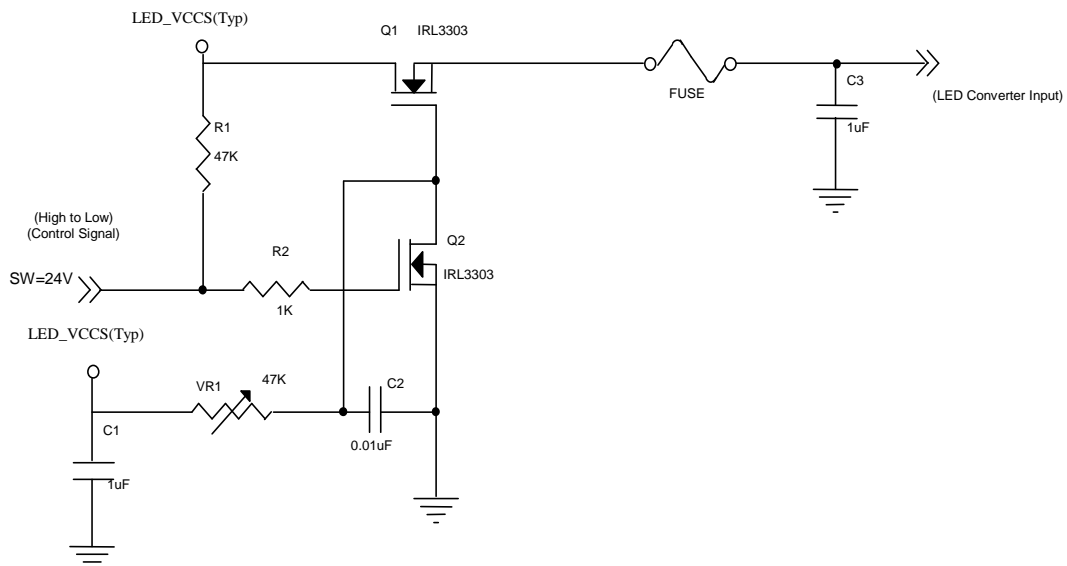
4.3.2 LED CONVERTER SPECIFICATION

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Converter Input power supply voltage		LED_Vccs	5.0	12.0	21.0	V	
Converter Inrush Current		I _{LED_RUSH}	-	-	1.5	A	(1)
EN Control Level	Backlight On		2.2	-	5	V	
	Backlight Off		0	-	0.6	V	
PWM Control Level	PWM High Level		2.2	-	5	V	
	PWM Low Level		0	-	0.6	V	
PWM Control Duty Ratio			5	-	100	%	
PWM Control Permissible Ripple Voltage		V _{PWM_pp}	-	-	100	mV	
PWM Control Frequency		f _{PWM}	190	-	2K	Hz	(2)
LED Power Current	LED_VCCS =Typ.	I _{LED}	81	101	113	mA	(3)

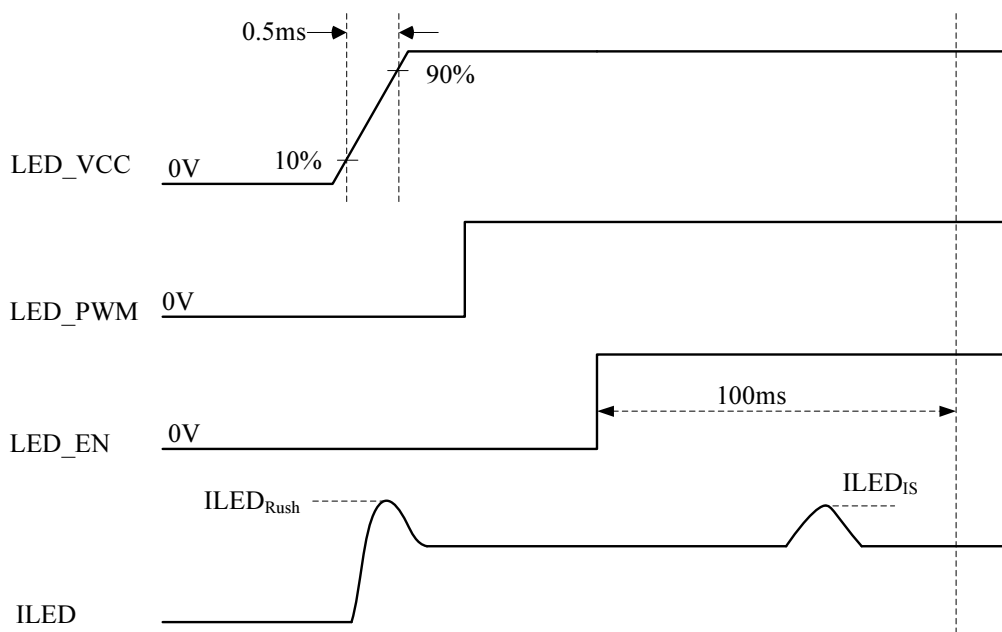
Note (1) I_{LED_RUSH}: the maximum current when LED_VCCS is rising,

I_{LED_IS}: the maximum current of the first 100ms after power-on,

Measurement Conditions: Shown as the following figure. LED_VCCS = Typ, Ta = 25 ± 2 °C, f_{PWM} = 200 Hz, Duty=100%.



VLED rising time is 0.5ms



Note (2) If PWM control frequency is applied in the range less than 1KHz, the “waterfall” phenomenon on the screen may be found. To avoid the issue, it’s a suggestion that PWM control frequency should follow the criterion as below.

PWM control frequency f_{PWM} should be in the range

$$(N + 0.33) * f \leq f_{PWM} \leq (N + 0.66) * f$$

N : Integer ($N \geq 3$)

f : Frame rate

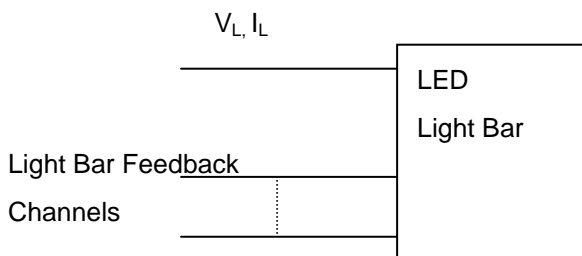
Note (3) The specified LED power supply current is under the conditions at “LED_VCCS = Typ.”, $T_a = 25 \pm 2 \text{ }^\circ\text{C}$, $f_{PWM} = 200 \text{ Hz}$, Duty=100%.

4.3.3 BACKLIGHT UNIT

Ta = 25 ± 2 °C

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
LED Light Bar Power Supply Voltage	V _L	26	28	30	V	(1)(2)(Duty100%)
LED Light Bar Power Supply Current	I _L		36		mA	
Power Consumption	P _L	0.936	1.008	1.08	W	(3)
LED Life Time	L _{BL}	15000	-	-	Hrs	(4)

Note (1) LED current is measured by utilizing a high frequency current meter as shown below :



Note (2) For better LED light bar driving quality, it is recommended to utilize the adaptive boost converter with current balancing function to drive LED light-bar.

Note (3) $P_L = I_L \times V_L$ (Without LED converter transfer efficiency)

Note (4) The lifetime of LED is defined as the time when it continues to operate under the conditions at Ta = 25 ± 2 °C and I_L = 20 mA(Per EA) until the brightness becomes ≤ 50% of its original value.

4.4 LVDS INPUT SIGNAL TIMING SPECIFICATIONS

4.4.1 DISPLAY PORT INTERFACE

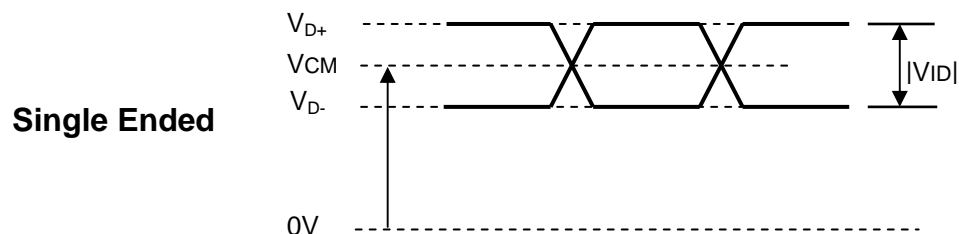
Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Differential Signal Common Mode Voltage(MainLink and AUX)	VCM	0		2	V	(1)(3)
AUX AC Coupling Capacitor	C _{AUX}	75		200	nF	(2)

Note (1) Display port interface related AC coupled signals should follow VESA DisplayPort Standard

Version1. Revision 1a and VESA Embedded DisplayPort™ Standard Version 1.2. There are many optional items described in eDP1.2. If some optional item is requested, please contact us.

(2) The AUX AC Coupling Capacitor should be placed on Source Devices.

(3)The source device should pass the test criteria described in DisplayPortCompliance Test Specification (CTS) 1.1



4.4.2 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 6-bit gray scale data input for the color. The higher the binary input the brighter the color. The table below provides the assignment of color versus data input.

Color		Data Signal																	
		Red						Green						Blue					
		R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(1)	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red(2)	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
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	Red(61)	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red(62)	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
Red(63)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	
Gray Scale Of Green	Green(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(1)	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
	Green(2)	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
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	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green(61)	0	0	0	0	0	0	1	1	1	1	0	1	0	0	0	0	0	0
	Green(62)	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0
Green(63)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	
Gray Scale Of Blue	Blue(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
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	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue(61)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1
	Blue(62)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0
Blue(63)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	

Note (1) 0: Low Level Voltage, 1: High Level Voltage

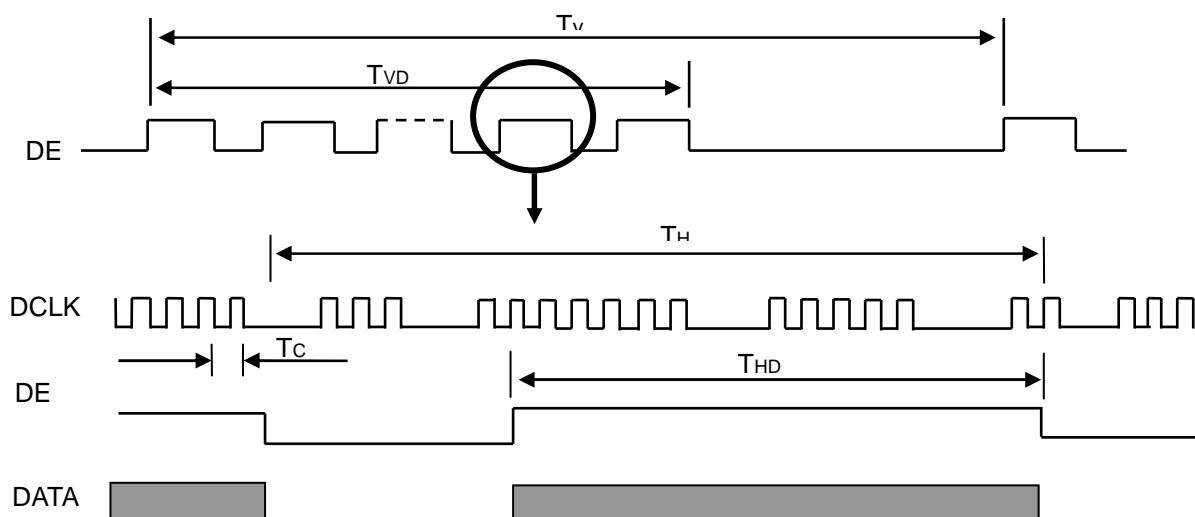
4.5 DISPLAY TIMING SPECIFICATIONS

The input signal timing specifications are shown as the following table and timing diagram.

Refresh rate 60Hz

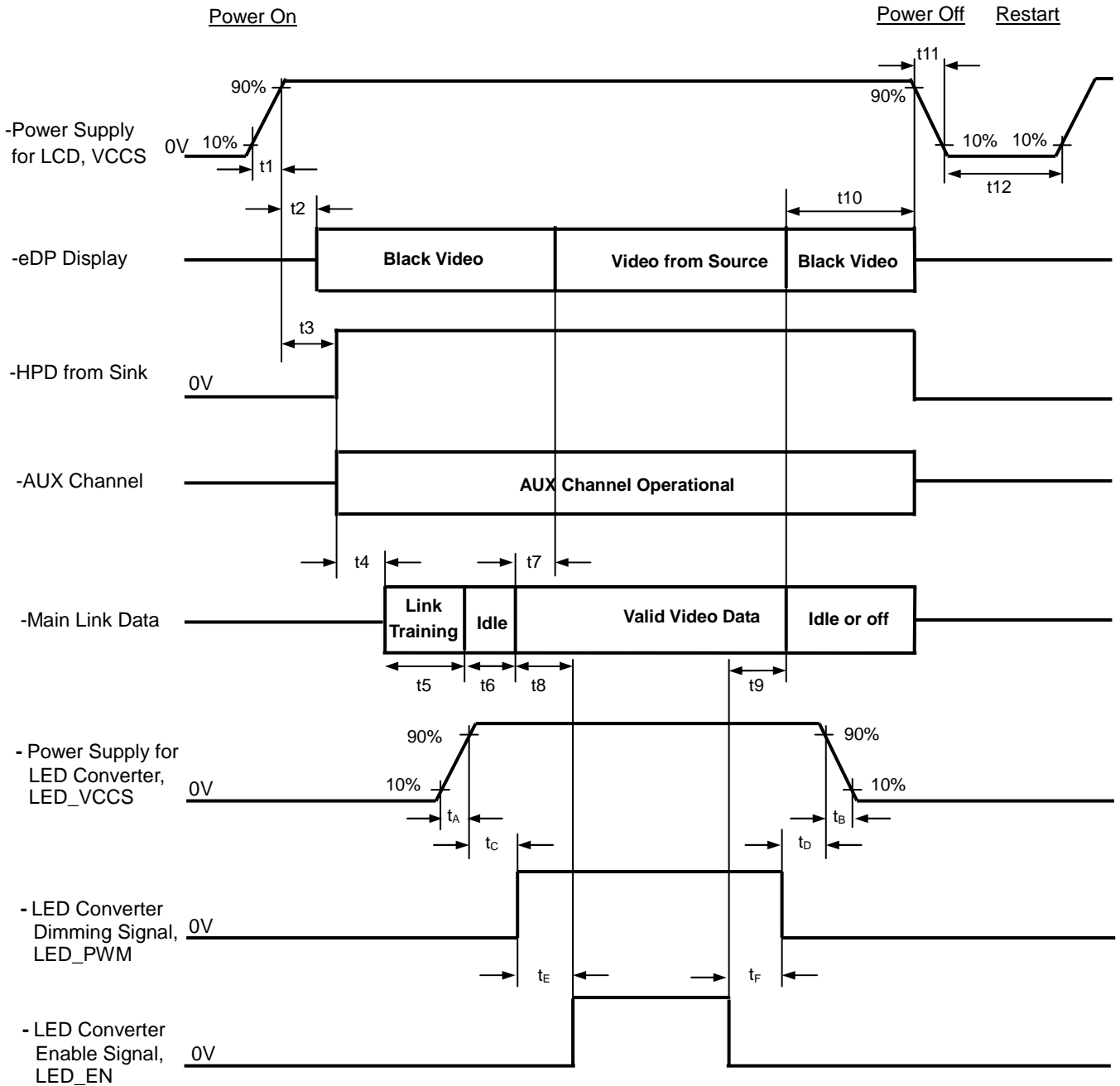
Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
DCLK	Frequency	1/Tc	67.9	75.45	79.22	MHz	-
DE	Vertical Total Time	TV	788	806	868	TH	-
	Vertical Active Display Period	TVD	768	768	768	TH	-
	Vertical Active Blanking Period	TVB	TV-TVD	38	TV-TVD	TH	-
	Horizontal Total Time	TH	1486	1560	1716	Tc	-
	Horizontal Active Display Period	THD	1366	1366	1366	Tc	-
	Horizontal Active Blanking Period	THB	TH-THB	194	TH-THB	Tc	-

INPUT SIGNAL TIMING DIAGRAM



4.6 POWER ON/OFF SEQUENCE

The power sequence specifications are shown as the following table and diagram.



Timing Specifications:

Parameter	Description	Reqd. By	Value		Unit	Notes
			Min	Max		
t1	Power rail rise time, 10% to 90%	Source	0.5	10	ms	-
t2	Delay from LCD,VCCS to black video generation	Sink	0	200	ms	Prevents display noise until valid video data is received from the Source
t3	Delay from LCD,VCCS to HPD high	Sink	0	200	ms	Sink Aux Channel must be operational upon HPD high
t4	Delay from HPD high to link training initialization	Source	-	-	ms	Allows for Source to read Link capability and initialize
t5	Link training duration	Source	-	-	ms	Dependant on Source link training protocol
t6	Link idle	Source	-	-	ms	Min accounts for required BS-Idle pattern. Max allows for Source frame synchronization
t7	Delay from valid video data from Source to video on display	Sink	0	50	ms	Max allows Sink validate video data and timing
t8	Delay from valid video data from Source to backlight on	Source	-	-	ms	Source must assure display video is stable
t9	Delay from backlight off to end of valid video data	Source	-	-	ms	Source must assure backlight is no longer illuminated
t10	Delay from end of valid video data from Source to power off	Source	0	500	ms	-
t11	VCCS power rail fall time, 90% to 10%	Source	0.5	10	ms	-
t12	VCCS Power off time	Source	500	-	ms	-
t _A	LED power rail rise time, 10% to 90%	Source	0.5	10	ms	-
t _B	LED power rail fall time, 90% to 10%	Source	0	10	ms	-
t _C	Delay from LED power rising to LED dimming signal	Source	1	-	ms	-
t _D	Delay from LED dimming signal to LED power falling	Source	1	-	ms	-
t _E	Delay from LED dimming signal to LED enable signal	Source	1	-	ms	-
t _F	Delay from LED enable signal to LED dimming signal	Source	1	-	ms	-

Note (1) Please don't plug or unplug the interface cable when system is turned on.

Note (2) Please avoid floating state of the interface signal during signal invalid period.

Note (3) It is recommended that the backlight power must be turned on after the power supply for LCD and the interface signal is valid.

5. OPTICAL CHARACTERISTICS

5.1 TEST CONDITIONS

Item	Symbol	Value	Unit
Ambient Temperature	T _a	25±2	°C
Ambient Humidity	H _a	50±10	%RH
Supply Voltage	V _{CC}	3.3	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
LED Light Bar Input Current	I _L	36	mA

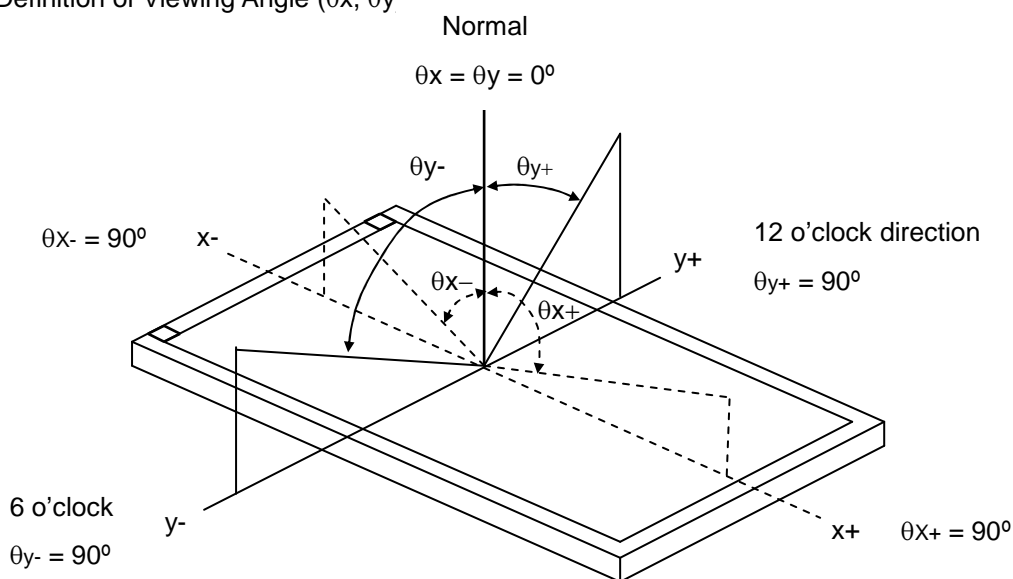
The measurement methods of optical characteristics are shown in Section 5.2. The following items should be measured under the test conditions described in Section 5.1 and stable environment shown in Note (6).

5.2 OPTICAL SPECIFICATIONS

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note			
Contrast Ratio	CR	$\theta_x=0^\circ, \theta_y=0^\circ$ Viewing Normal Angle	500	650		-	(2), (6), (9)			
Response Time	T _R			3	8	ms	(3), (9)			
	T _F			8	13	ms				
Average Luminance of White (5 points)	Y _{LAVE}			255	300		cd/m ²	(4), (6), (9)		
Cross Modulation	D				2	%	(5), (9)			
Color Chromaticity	Red		R _x	Typ - 0.03	0.595	Typ + 0.03	-	(1), (9)		
			R _y		0.345		-			
	Green		G _x		0.320		-			
			G _y		0.565		-			
	Blue		B _x		0.155		-			
		B _y	0.130		-					
	White	W _x	0.283		0.313		0.343		-	
		W _y	0.299		0.329		0.359		-	
Viewing Angle	Horizontal	θ_{x+}	CR≥10	40	45	Deg.	(1), (6), (9)			
		θ_{x-}		40	45					
	Vertical	θ_{y+}		15	20					
		θ_{y-}		40	45					
	Horizontal	θ_{x+}		CR≥5	50			55	Deg.	(1), (6), (9)
		θ_{x-}			50			55		
Vertical	θ_{y+}	25	30							
	θ_{y-}	50	55							
13 Points White Variation	θ_{y-}	$\theta_x=0^\circ, \theta_y=0^\circ$ Viewing normal angle			1.55	1.67		(7), (8), (9)		
13 Point CR Variation	δW				1.43	2.0				
White Variation	δC_R			2.0	5.0	%/mm				
Gamma	63	$\theta_x=0^\circ, \theta_y=0^\circ$ Viewing normal angle	100	100	100	%	(6), (9)			
	60		87.7	89.8	92.0					
	56		72.8	77.2	81.9					
	52		59.6	65.6	72.2					
	48		48.0	55.0	63.0					
	44		37.9	45.4	54.3					
	36		22.1	29.2	38.6					

	32		16.1	22.5	31.6		
	24		7.4	12.0	19.4		
	20		4.5	8.0	14.2		
	16		2.5	4.9	9.7		
	12		1.1	2.6	6.0		
	8		0.4	1.1	3.0		
	4		0.1	0.2	0.9		
	0		0	0	0		

Note (1) Definition of Viewing Angle (θ_x, θ_y)



Note (2) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

$$\text{Contrast Ratio (CR)} = L_{63} / L_0$$

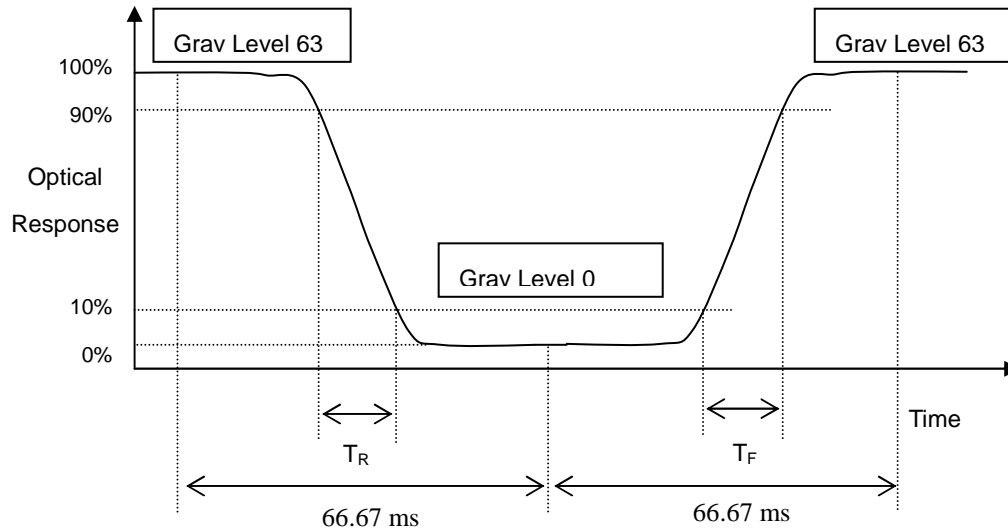
L63: Luminance of gray level 63

L0: Luminance of gray level 0

$$\text{CR} = \text{CR} (1)$$

CR (X) is corresponding to the Contrast Ratio of the point X at Figure in Note (6).

Note (3) Definition of Response Time (T_R, T_F):



Note (4) Definition of Average Luminance of White (L_{AVE}):

Measure the luminance of gray level 63 at 5 points

$$L_{AVE} = [L(1) + L(2) + L(3) + L(4) + L(5)] / 5$$

$L(x)$ is corresponding to the luminance of the point X at Figure in Note (6)

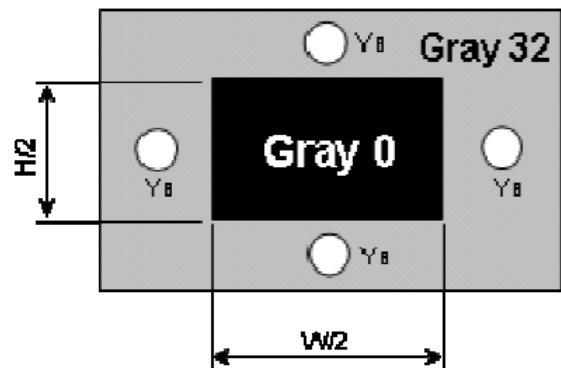
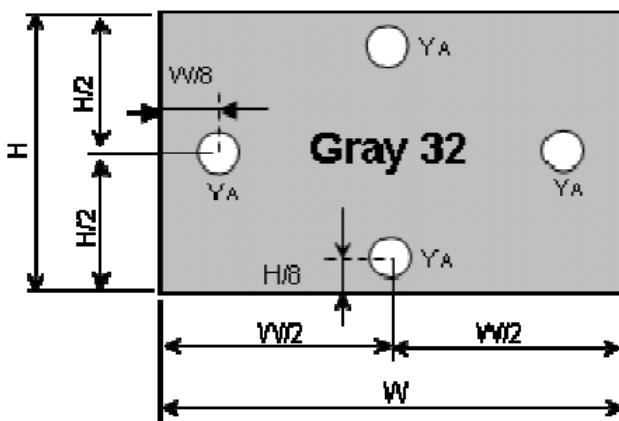
Note (5) Definition of Cross Modulation (D_{SHA})

$$D_{SHA} = |Y_B - Y_A| / Y_A \times 100\%$$

Where:

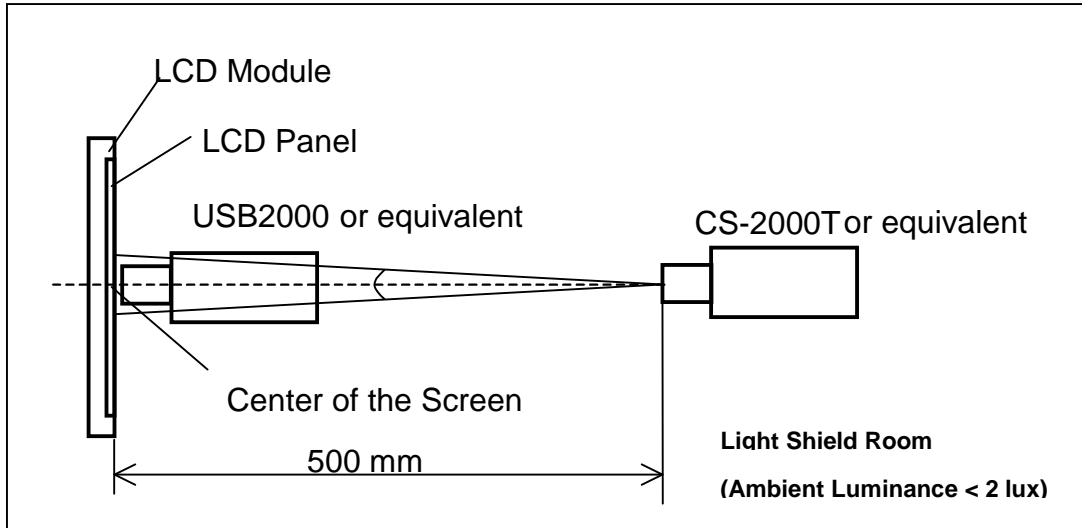
Y_A = Luminance of measured location without darkest gray pattern (cd/m^2)

Y_B = Luminance of measured location with darkest gray pattern (cd/m^2)



Note (6) Measurement Setup:

The LCD module should be stabilized at given temperature for 20 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 20 minutes in a windless room.

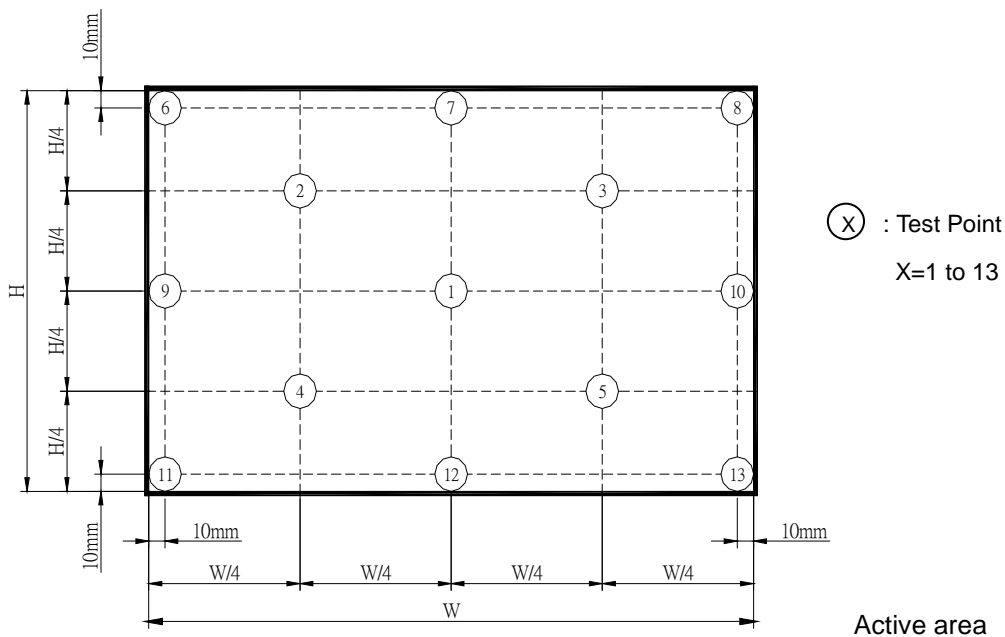


Note (7) Definition of White Variation (δW):

Measure the luminance of gray level 63 at 5 points

$$\delta W_{5p} = \{ \text{Minimum} [L(1) \sim L(5)] / \text{Maximum} [L(1) \sim L(5)] \} * 100\%$$

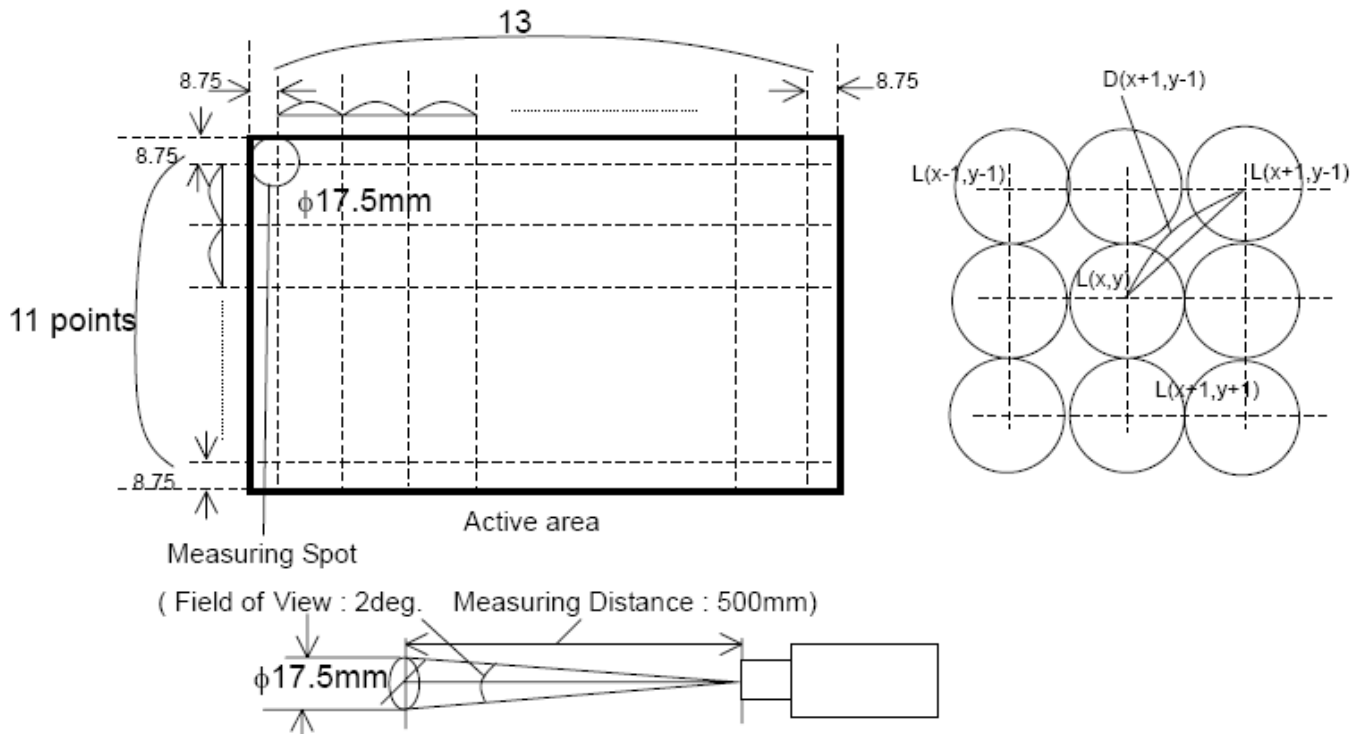
$$\delta W_{13p} = \{ \text{Minimum} [L(1) \sim L(13)] / \text{Maximum} [L(1) \sim L(13)] \} * 100\%$$



Note (8) Definition of White Variation dL : measure the luminance of white at 13×11 points.

$$dL = |L(x,y) - L(x+l, y+j)| / (L(x,y) \times D(x+l, y+j)) \times 100 \quad (\%/mm)$$

where $2 \leq x \leq 12, \quad 2 \leq y \leq 10, l = \pm 1, \quad j = \pm 1$



Note (9) The listed optical specifications refer to the initial value of manufacture, but the condition of the specifications after long-term operation will not be warranted.

6. RELIABILITY TEST ITEM

Test Item	Test Condition	Note
Mechanical Vibration	Frequency Range 5-500 Hz, 14.7m/s ² (1.5G) constant, 0.5Hrs each axis (X,Y,Z direction)	Non Operation
	Frequency Range 5-500 Hz, 4.9 m/s ² (0.5G) constant, 0.5Hrs each axis (X,Y,Z direction)	Operation
Mechanical Shock	686m/s ² (70G), Pulse width 11ms, Half-Sine Wave,±X, ±Y, ±Z direction, each 3 times	Operation and Non Operation
	2548 m/s ² (260G), Pulse width 2ms, Half-Sine Wave,±X, ±Y, ±Z direction, each 1 times	
Pressure Resistance	A load of 180 Newtons (40lbf) is applied along the perimeter and a load of 270 Newtons (60lbf) is applied to the inner portion of the backside of and LCD to simulate the loading on the panel when assembled into a notebook computer. The load is applied over a 50mm x 50mm square area.	
Connector tension test	Input connector: With 50 times of connector trial there must be no damage to the shape and functional.	
	Back light connector: With 50 times of connector trial there must be no damage to the shape and functional.	

Note (1) criteria : Normal display image with no obvious non-uniformity and no line defect.

Note (2) Evaluation should be tested after storage at room temperature for more than two hour

Note (3) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.

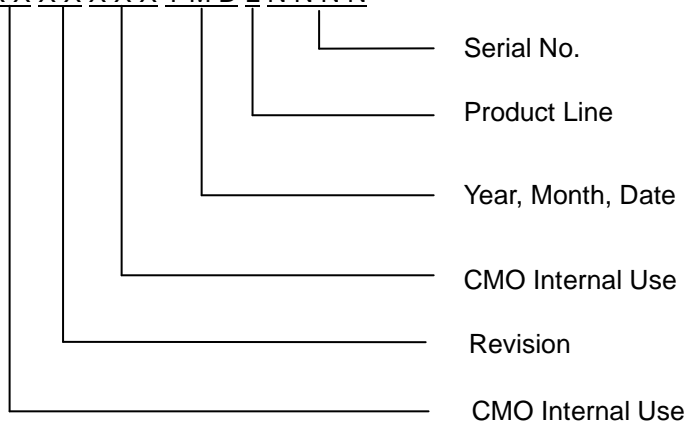
7. PACKING

7.1 MODULE LABEL

The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.



- (a) Model Name: N133BGE - EB1
- (b) Revision: Rev. XX, for example: C1, C2 ...etc.
- (c) Serial ID: X X X X X X Y M D L N N N N



Serial ID includes the information as below:

- (a) Manufactured Date: Year: 0~9, for 2010~2019
 Month: 1~9, A~C, for Jan. ~ Dec.
 Day: 1~9, A~Y, for 1st to 31st, exclude I , O and U
- (b) Revision Code: cover all the change
- (c) Serial No.: Manufacturing sequence of product
- (d) Product Line: 1 -> Line1, 2 -> Line 2, ...etc.

7.2 CARTON

Box Dimensions : 540(L)*450(W)*275(H)
Weight : Approx. 10.93Kg (40 module .per. 1box)

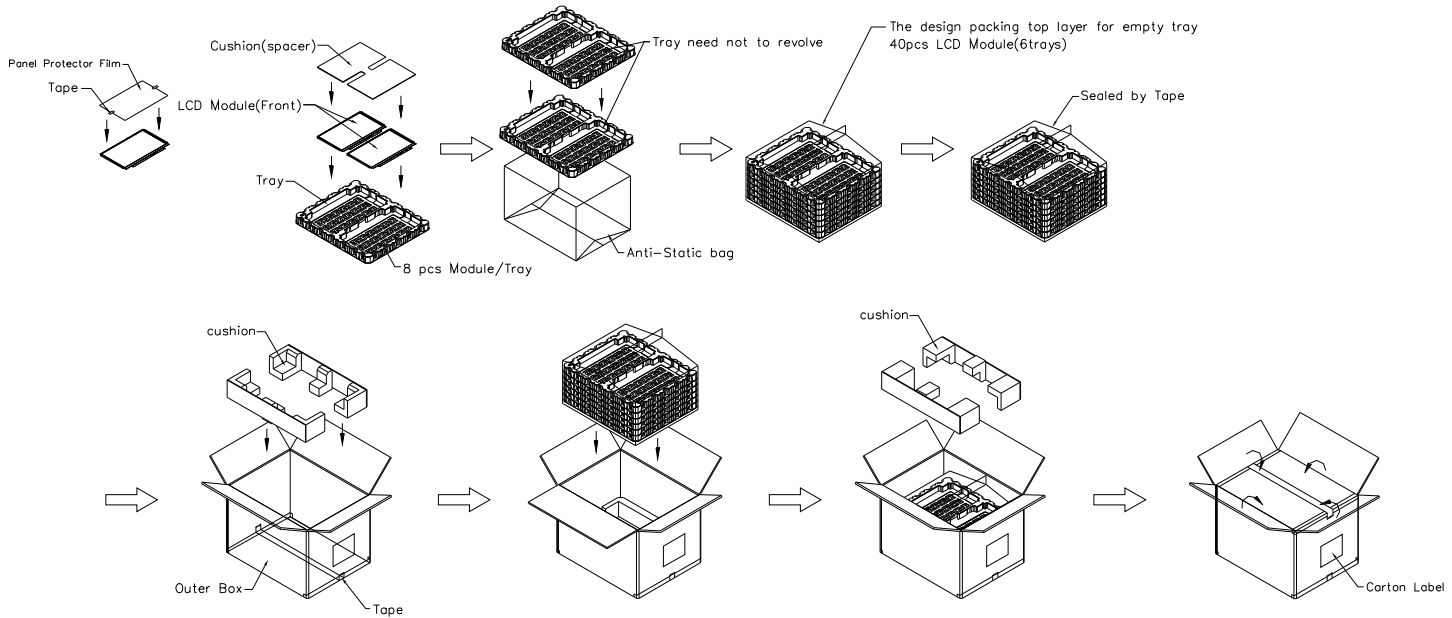


Figure. 7-2 Packing

7.3 PALLET

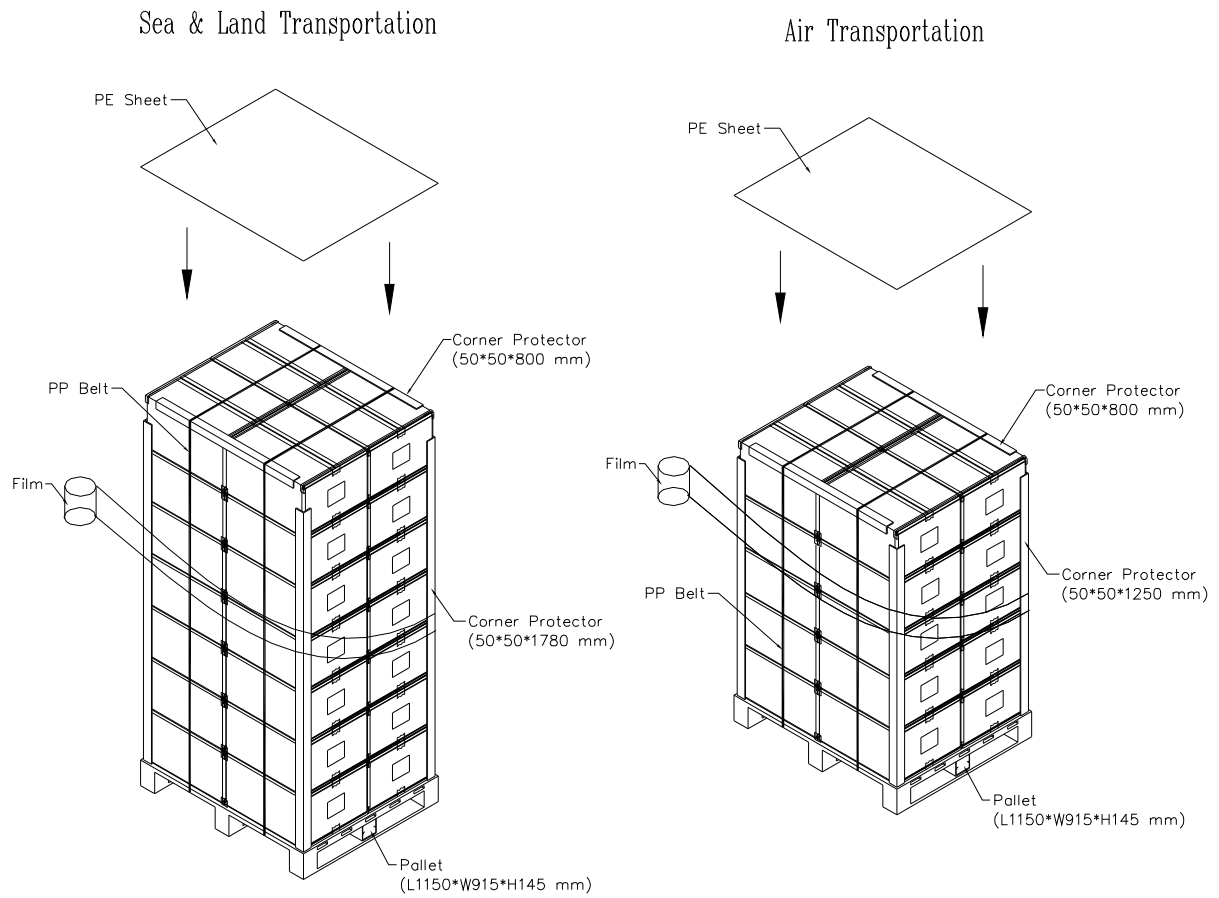


Figure. 7-3 Packing

8. PRECAUTIONS

8.1 HANDLING PRECAUTIONS

- (1) The module should be assembled into the system firmly by using every mounting hole. Be careful not to twist or bend the module.
- (2) While assembling or installing modules, it can only be in the clean area. The dust and oil may cause electrical short or damage the polarizer.
- (3) Use fingerstalls or soft gloves in order to keep display clean during the incoming inspection and assembly process.
- (4) Do not press or scratch the surface harder than a HB pencil lead on the panel because the polarizer is very soft and easily scratched.
- (5) If the surface of the polarizer is dirty, please clean it by some absorbent cotton or soft cloth. Do not use Ketone type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanently damage the polarizer due to chemical reaction.
- (6) Wipe off water droplets or oil immediately. Staining and discoloration may occur if they left on panel for a long time.
- (7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contacting with hands, legs or clothes, it must be washed away thoroughly with soap.
- (8) Protect the module from static electricity, it may cause damage to the C-MOS Gate Array IC.
- (9) Do not disassemble the module.
- (10) Do not pull or fold the LED wire.
- (11) Pins of I/F connector should not be touched directly with bare hands.

8.2 STORAGE PRECAUTIONS

- (1) High temperature or humidity may reduce the performance of module. Please store LCD module within the specified storage conditions.
- (2) It is dangerous that moisture come into or contacted the LCD module, because the moisture may damage LCD module when it is operating.
- (3) It may reduce the display quality if the ambient temperature is lower than 10 °C. For example, the response time will become slowly, and the starting voltage of LED will be higher than the room temperature.

8.3 OPERATION PRECAUTIONS

- (1) Do not pull the I/F connector in or out while the module is operating.
- (2) Always follow the correct power on/off sequence when LCD module is connecting and operating. This can prevent the CMOS LSI chips from damage during latch-up.
- (3) The startup voltage of Backlight is approximately 1000 Volts. It may cause electrical shock while assembling with converter. Do not disassemble the module or insert anything into the Backlight unit.

Appendix. EDID DATA STRUCTURE

The EDID (Extended Display Identification Data) data formats are to support displays as defined in the VESA Plug & Display and FPD standards.

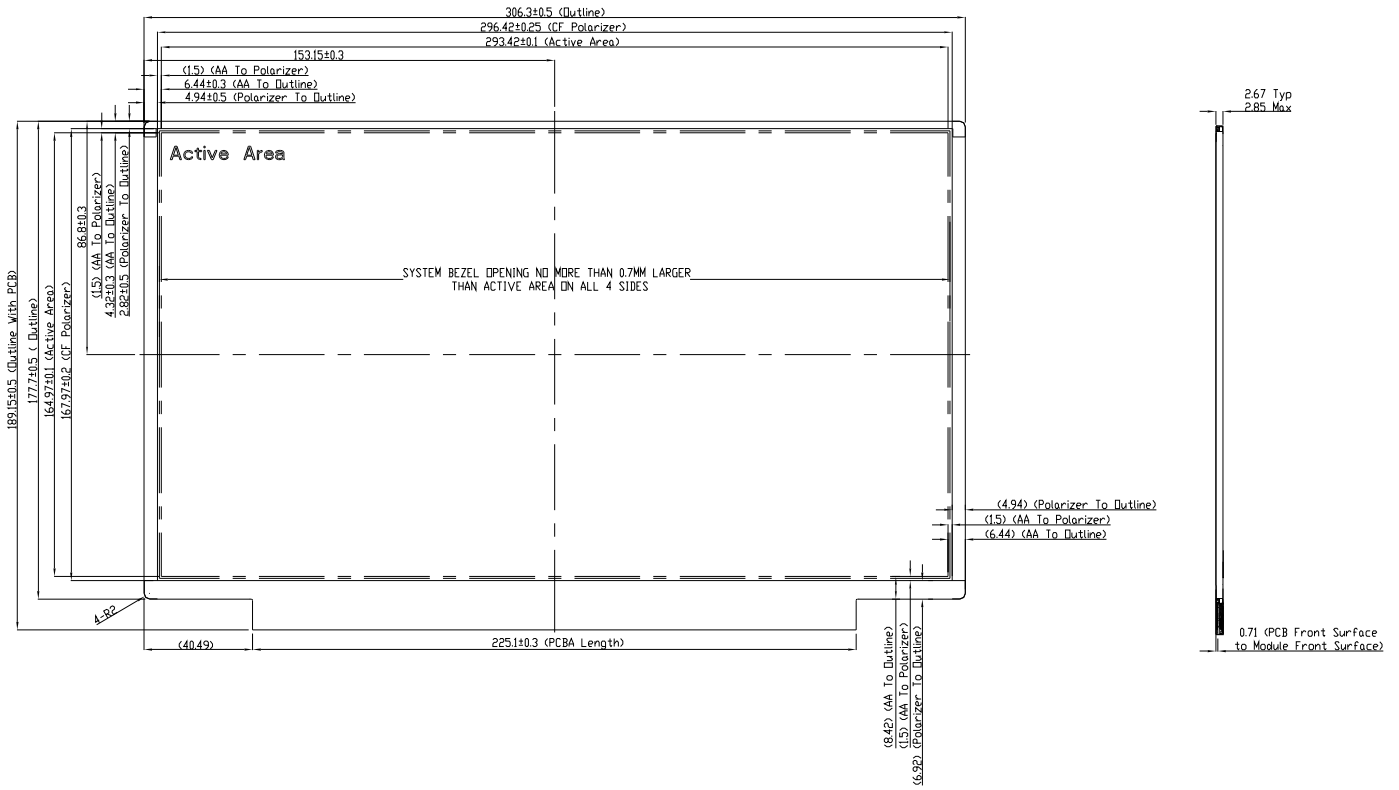
Byte # (decimal)	Byte # (hex)	Field Name and Comments	Value (hex)	Value (binary)
0	0	Header	00	00000000
1	1	Header	FF	11111111
2	2	Header	FF	11111111
3	3	Header	FF	11111111
4	4	Header	FF	11111111
5	5	Header	FF	11111111
6	6	Header	FF	11111111
7	7	Header	00	00000000
8	8	EISA ID manufacturer name ("CMN")	0D	00001101
9	9	EISA ID manufacturer name (Compressed ASCII)	AE	10101110
10	0A	ID product code (N133BGE-EB1)	50	01010000
11	0B	ID product code (hex LSB first; N133BGE-EB1)	13	00010011
12	0C	ID S/N (fixed "0")	00	00000000
13	0D	ID S/N (fixed "0")	00	00000000
14	0E	ID S/N (fixed "0")	00	00000000
15	0F	ID S/N (fixed "0")	00	00000000
16	10	Week of manufacture (fixed week code)	28	00101000
17	11	Year of manufacture (fixed year code)	16	00010110
18	12	EDID structure version # ("1")	01	00000001
19	13	EDID revision # ("4")	04	00000100
20	14	Video I/P definition ("digital")	95	10010101
21	15	Max H image size ("30.68cm")	1F	00011111
22	16	Max V image size ("17.82cm")	12	00010010
23	17	Display Gamma (Gamma = "2.2")	78	01111000
24	18	Feature support ("Active off, RGB Color")	02	00000010
25	19	Rx1, Rx0, Ry1, Ry0, Gx1, Gx0, Gy1, Gy0	53	01010011
26	1A	Bx1, Bx0, By1, By0, Wx1, Wx0, Wy1, Wy0	D5	11010101
27	1B	Rx=0.595	98	10011000
28	1C	Ry=0.345	58	01011000
29	1D	Gx=0.32	52	01010010
30	1E	Gy=0.565	90	10010000
31	1F	Bx=0.155	27	00100111
32	20	By=0.13	21	00100001
33	21	Wx=0.313	50	01010000
34	22	Wy=0.329	54	01010100
35	23	Established timings 1	00	00000000
36	24	Established timings 2	00	00000000
37	25	Manufacturer's reserved timings	00	00000000
38	26	Standard timing ID # 1	01	00000001
39	27	Standard timing ID # 1	01	00000001
40	28	Standard timing ID # 2	01	00000001
41	29	Standard timing ID # 2	01	00000001

42	2A	Standard timing ID # 3	01	00000001
43	2B	Standard timing ID # 3	01	00000001
44	2C	Standard timing ID # 4	01	00000001
45	2D	Standard timing ID # 4	01	00000001
46	2E	Standard timing ID # 5	01	00000001
47	2F	Standard timing ID # 5	01	00000001
48	30	Standard timing ID # 6	01	00000001
49	31	Standard timing ID # 6	01	00000001
50	32	Standard timing ID # 7	01	00000001
51	33	Standard timing ID # 7	01	00000001
52	34	Standard timing ID # 8	01	00000001
53	35	Standard timing ID # 8	01	00000001
54	36	Detailed timing description # 1 Pixel clock ("75.45MHz", According to VESA CVT Rev1.1)	79	01111001
55	37	# 1 Pixel clock (hex LSB first)	1D	00011101
56	38	# 1 H active ("1366")	56	01010110
57	39	# 1 H blank ("194")	C2	11000010
58	3A	# 1 H active : H blank ("1366 : 194")	50	01010000
59	3B	# 1 V active ("768")	00	00000000
60	3C	# 1 V blank ("38")	26	00100110
61	3D	# 1 V active : V blank ("768 :38")	30	00110000
62	3E	# 1 H sync offset ("31")	1F	00011111
63	3F	# 1 H sync pulse width ("65")	41	01000001
64	40	# 1 V sync offset : V sync pulse width ("4 : 12")	4C	01001100
65	41	# 1 H sync offset : H sync pulse width : V sync offset : V sync width ("31: 65 : 4 : 12")	00	00000000
66	42	# 1 H image size ("344 mm")	58	01011000
67	43	# 1 V image size ("194 mm")	C2	11000010
68	44	# 1 H image size : V image size ("344 : 194")	10	00010000
69	45	# 1 H boarder ("0")	00	00000000
70	46	# 1 V boarder ("0")	00	00000000
71	47	# 1 Non-interlaced, Normal, no stereo, Separate sync, H/V pol Negatives	18	00011000
72	48	Detailed timing description # 2	00	00000000
73	49	# 2 Flag	00	00000000
74	4A	# 2 Reserved	00	00000000
75	4B	# 2 FE (hex) defines ASCII string (Model Name "N133BGE-EB1", ASCII)	FE	11111110
76	4C	# 2 Flag	00	00000000
77	4D	# 2 1st character of name ("N")	4E	01001110
78	4E	# 2 2nd character of name ("1")	31	00110001
79	4F	# 2 3rd character of name ("3")	33	00110011
80	50	# 2 4th character of name ("3")	33	00110011
81	51	# 2 5th character of name ("B")	42	01000010
82	52	# 2 6th character of name ("G")	47	01000111
83	53	# 2 7th character of name ("E")	45	01000101
84	54	# 2 8th character of name ("-")	2D	00101101
85	55	# 2 9th character of name ("E")	45	01000101

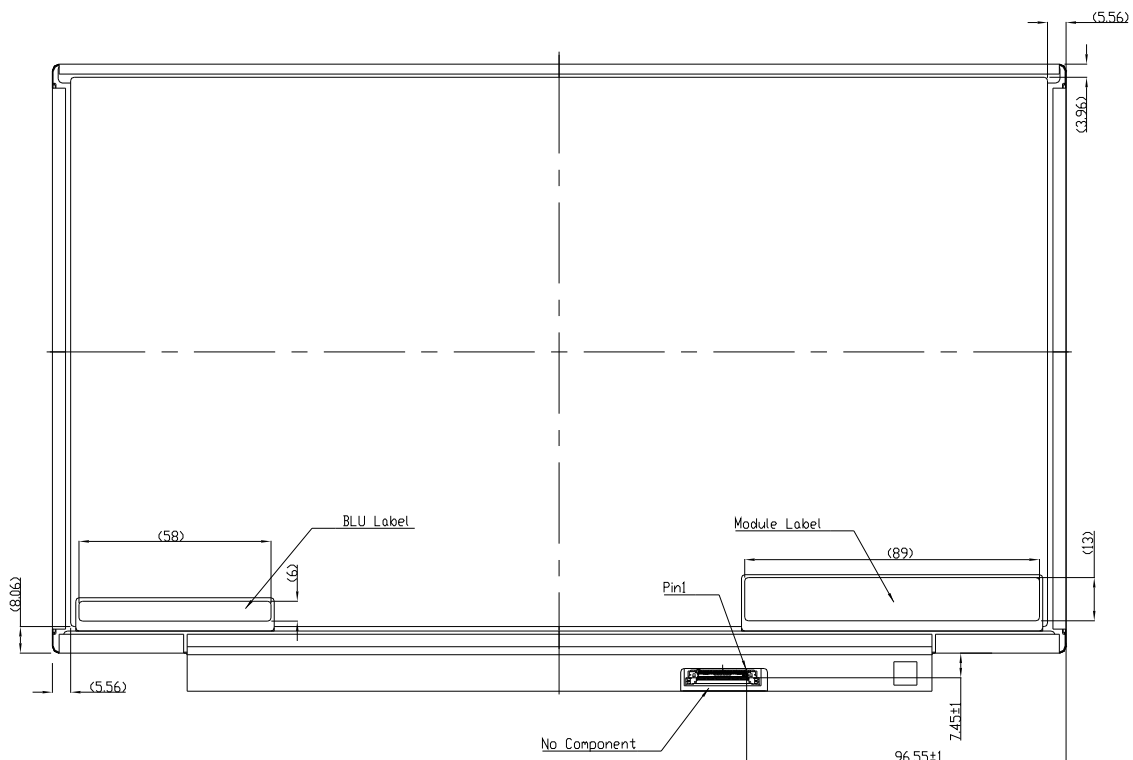
Byte # (decimal)				
	56	# 2 10th character of name ("B")	42	01000010
86	57	# 2 11th character of name ("1")	31	00110001
87	58	# 2 Padding with "Blank" character	20	00100000
88	59	# 2 Padding with "Blank" character	20	00100000
89	5A	Detailed timing description # 3	00	00000000
90	5B	# 3 Flag	00	00000000
91	5C	# 3 Reserved	00	00000000
92	5D	# 3 FE (hex) defines ASCII string (Vendor "CMN", ASCII)	FE	11111110
93	5E	# 3 Flag	00	00000000
94	5F	# 3 1st character of string ("C")	43	01000011
95	60	# 3 2nd character of string ("M")	4D	01001101
96	61	# 3 3rd character of string ("N")	4E	01001110
97	62	# 3 New line character indicates end of ASCII string	0A	00001010
98	63	# 3 Padding with "Blank" character	20	00100000
99	64	# 3 Padding with "Blank" character	20	00100000
100	65	# 3 Padding with "Blank" character	20	00100000
101	66	# 3 Padding with "Blank" character	20	00100000
102	67	# 3 Padding with "Blank" character	20	00100000
103	68	# 3 Padding with "Blank" character	20	00100000
104	69	# 3 Padding with "Blank" character	20	00100000
105	6A	# 3 Padding with "Blank" character	20	00100000
106	6B	# 3 Padding with "Blank" character	20	00100000
107	6C	Detailed timing description # 4	00	00000000
108	6D	# 4 Flag	00	00000000
109	6E	# 4 Reserved	00	00000000
110	6F	# 4 FE (hex) defines ASCII string (Model Name "N133BGE-EB1", ASCII)	FE	11111110
111	70	# 4 Flag	00	00000000
112	71	# 2 1st character of name ("N")	4E	01001110
113	72	# 2 2nd character of name ("1")	31	00110001
114	73	# 2 3rd character of name ("3")	33	00110011
115	74	# 2 4th character of name ("3")	33	00110011
116	75	# 2 5th character of name ("B")	42	01000010
117	76	# 2 6th character of name ("G")	47	01000111
118	77	# 2 7th character of name ("E")	45	01000101
119	78	# 2 8th character of name ("-")	2D	00101101
120	79	# 2 9th character of name ("E")	45	01000101
121	7A	# 2 10th character of name ("B")	42	01000010
122	7B	# 2 11th character of name ("1")	31	00110001
123	7C	# 4 Padding with "Blank" character	20	00100000
124	7D	# 4 Padding with "Blank" character	20	00100000
125	7E	Extension flag	00	00000000
126	7F	Checksum	7B	01111011

Appendix. OUTLINE DRAWING

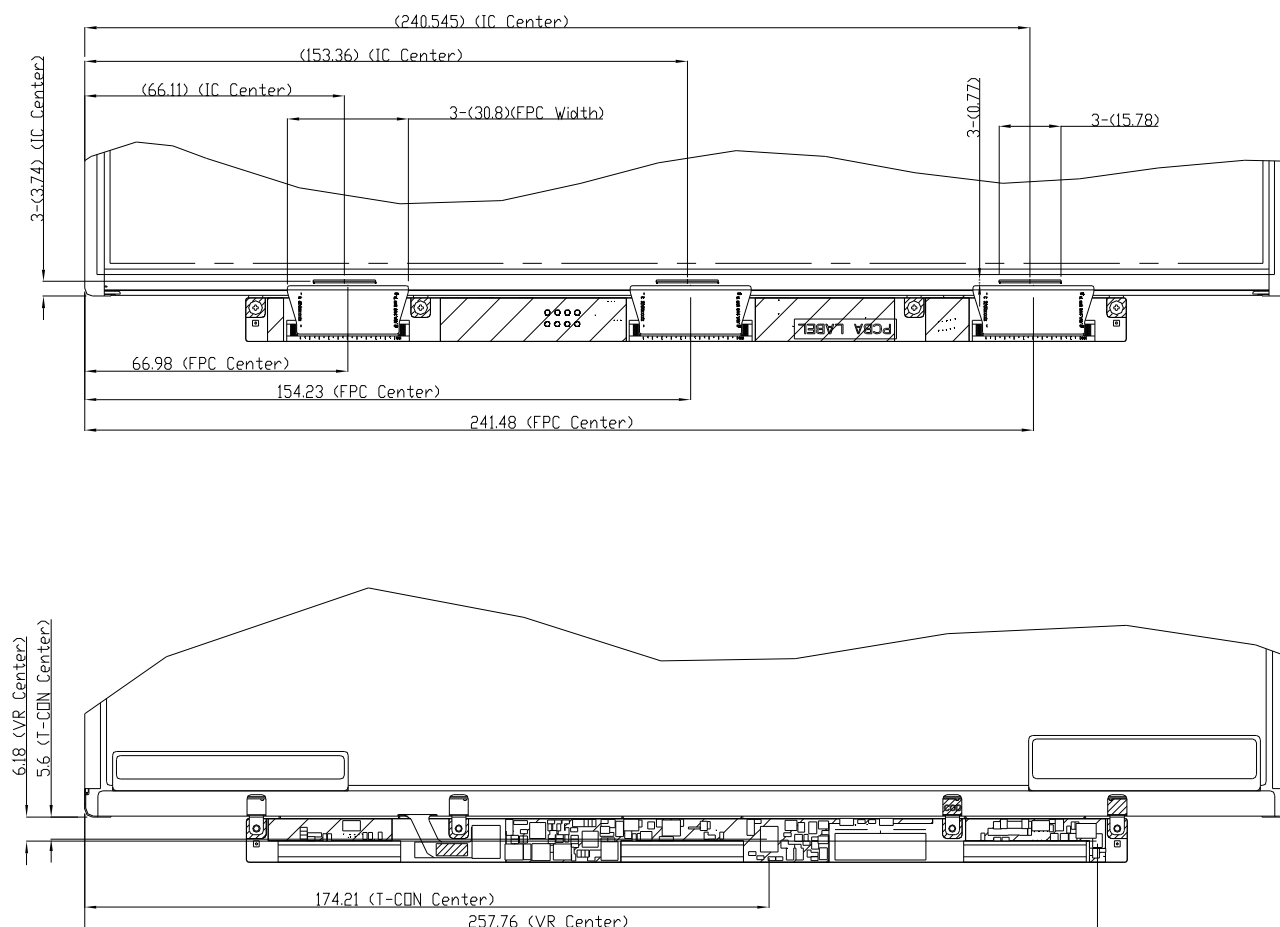
Front



Back



FPC Location



DRIVER IC, FPC, TCON, AND VR LOCATIONS
SEE NOTES FOR EXPLANATION

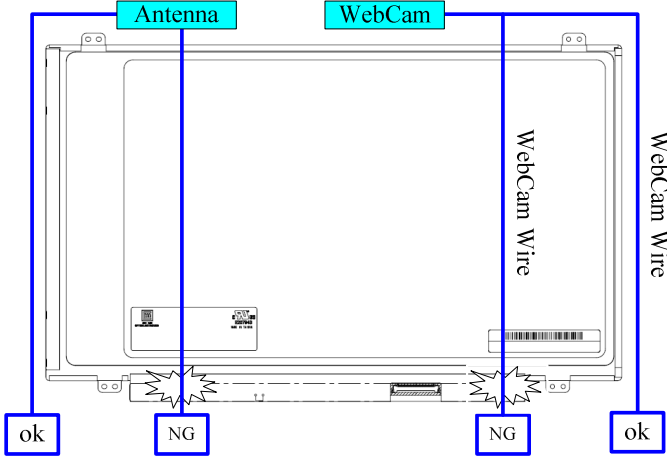
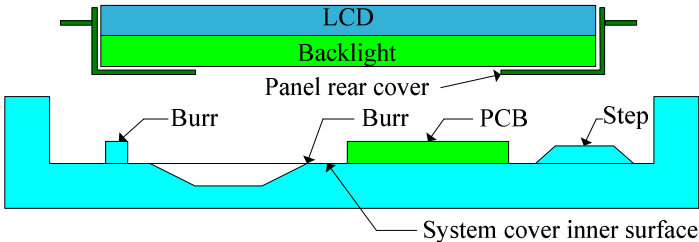
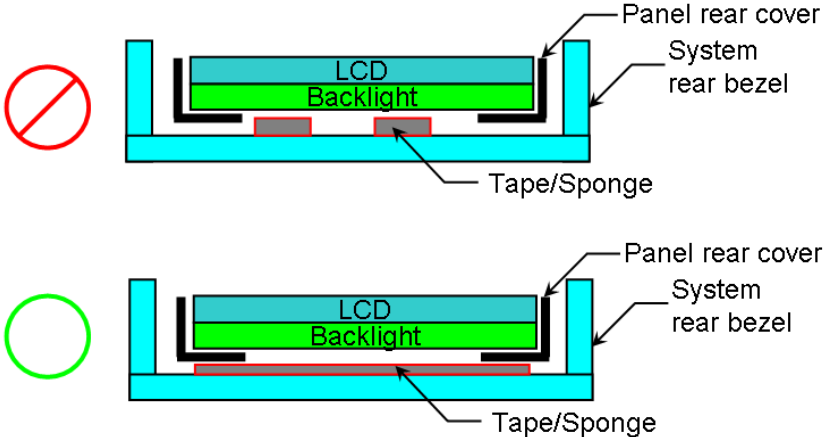
NOTES:

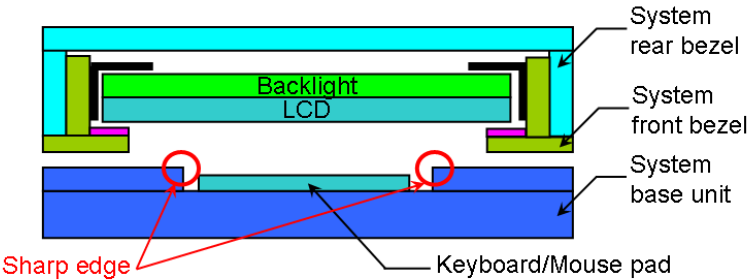
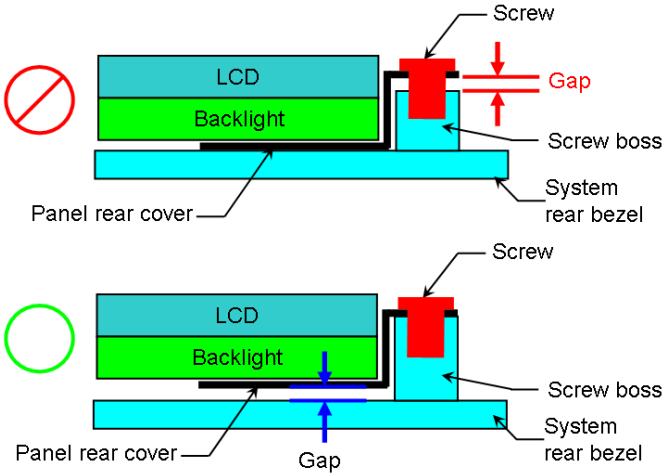
1. FLATNESS 1.5 mm MAX
2. "< >" MARK THE REFERENCE DIMENSIONS
3. LCD MODULE INPUT CONNECTOR: I-PEX:20455-030E-12, TYCD:5-2069716-2
4. IN ORDER TO AVOID ABNORMAL DISPLAY, POOLING AND WHITE SPOT, NO OVERLAPPING IS SUGGESTED AT CABLES, ANTENNAS CAMERA, WLAN, WAM OR OTHER FOREIGN OBJECTS OVER FPC DRIVER IC, TCON AND VR LOCATION.
5. LVDS CONNECTOR IS MEASURED AT PIN1 AND ITS MATING LINE.

Appendix. SYSTEM COVER DESIGN GUIDANCE

<p>1.</p>	<p>Design gap A between panel & any components on system cover</p>
<p>Definition</p>	<p>a). At least 0.5mm gap between panel & system is recommended for preventing from backpack or pogo test fail.</p> <p>b). Zero gap from panel's maximum thickness boundary to any components, foreign objects, wire, cable or extrusion on system cover inner surface is forbidden.</p>
<p>2</p>	<p>Design gap B1 & B2 between panel & protrusions</p>
<p>Definition</p>	<p>2.0mm min. gap is recommended between panel & protrusions for preventing from shock related failures.</p>

3	Design gap C between system front bezel & panel surface.
Definition	<p>a). Sufficient gap between system front bezel & panel surface is a must for preventing from pooling or glass broken.</p> <p>b). Zero gap or interference is forbidden.</p> <p>c). Zero gap is also forbidden in the act of system front bezel deformation during swing test, hinge test, knock test, or during pooling inspection procedure.</p> <p>d). To remain sufficient gap, design with system rib higher than maximum panel thickness is recommended.</p>
4	Design gap D1 & D2 between system front bezel & PCB Assembly.
Definition	<p>a). Sufficient gap between system front bezel & PCB assembly is a must for preventing from abnormal display after backpack test, hinge test, twist test or pogo test.</p> <p>b). Zero gap or interference is forbidden.</p> <p>c). Zero gap is also forbidden in the act of system front bezel deformation during hinge test, twist test, or during pooling inspection procedure.</p> <p>d). To remain sufficient gap, design with system rib higher than maximum panel thickness is recommended.</p>

5	<p>Interference examination of antenna cable and WebCam wire</p> 
Definition	<p>a). Antenna cable or WebCam wire overlap with panel outline is forbidden for preventing from abnormal display & white spot after backpack test, hinge test, twist test or pogo test.</p> <p>b). Antenna cable or WebCam wire bypass panel outline is recommended.</p>
6	<p>System inner surface examination</p> 
Definition	<p>a). Burr at logo edge, step, protrusion or PCB board will easily cause white spot or glass broken.</p> <p>b). Keeping flat surface underneath backlight is recommended.</p>
7	<p>Tape/sponge design on system inner surface</p> 

<p>Definition</p>	<p>a) To prevent abnormal display & white spot after scuffing test, hinge test, pogo test, backpack test, as the poor rigidity result from deformation of system rear cover during the test.</p> <p>b) We suggest using aluminum-magnesium alloy as the rear frame material with thickness min 1.5mm, instead of using PC/ABS.</p>
<p>11</p>	<p>System base unit design near keyboard and mouse pad</p>
	
<p>Definition</p>	<p>To prevent abnormal display & white spot after scuffing test, hinge test, pogo test, backpack test, no sharp edge design is allowed in any area that may damage the panel during the test. We suggest to remove all sharp edges, or to reduce the thickness difference of keyboard/mouse pad from the nearby surface.</p>
<p>12</p>	<p>Screw boss height design</p>
	
<p>Definition</p>	<p>a). Gap left between panel rear cover bracket and screw boss surface is prohibited.</p> <p>b). To remain sufficient gap between panel and system rear bezel, screw boss height must be designed with respect to the height of bracket bottom surface to panel bottom surface + flatness change of panel itself.</p>